CLAIMS

What is claimed is:

1. A multilayer substrate for mounting a die comprising:

a ceramic portion comprising an embedded capacitor having first and second terminals;

a first plurality of lands on a first surface thereof, including a first land coupled to the first terminal and a second land coupled to the second terminal, wherein the first and second lands are positioned to be coupled to corresponding power supply nodes of the die; and

an organic portion comprising a plurality of conductors, including a first conductor coupling the first land to the first terminal and a second conductor coupling the second land to the second terminal.

2. The multilayer substrate recited in claim 1 and further comprising a second plurality of lands on a second surface thereof, including a third land coupled to the first terminal and a fourth land coupled to the second terminal.

3. The multilayer substrate recited in claim 2, wherein the pitch of the second plurality of lands is greater than the pitch of the first plurality of lands, and wherein the pitch is increased within the organic layer.

4. The multilayer substrate recited in claim 2, wherein the first plurality of lands further comprises a fifth land positioned to be coupled to a corresponding signal node of the die, and wherein the second plurality of lands comprises a sixth land coupled to the fifth land via a conductive path that comprises one of the plurality of conductors.

5. The multilayer substrate recited in claim 4, wherein the pitch of the second plurality of lands is greater than the pitch of the first plurality of lands, and wherein the pitch is increased within the organic layer.

6. The multilayer substrate recited in claim 2, wherein the third and fourth lands are positioned to be coupled to corresponding power supply nodes of an additional substrate subjacent to the multilayer ceramic substrate.

7. The multilayer substrate recited in claim 1, wherein the capacitor comprises at least one high permittivity layer.

8. The multilayer substrate recited in claim 1, wherein the capacitor comprises a plurality of high permittivity layers.

9. The multilayer substrate recited in claim 8, wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second lands, respectively.

10. The multilayer substrate recited in claim 1, wherein the organic portion comprises a plurality of layers, each comprising a portion of the plurality of conductors.

11. An electronic assembly comprising:

a multilayer substrate comprising:

a ceramic portion comprising an embedded capacitor having first and second terminals;

a first plurality of lands on a first surface thereof, including a first land coupled to the first terminal and a second land coupled to the second terminal; and

an organic portion comprising a plurality of conductors, including a first conductor coupling the first land to the first terminal and a second conductor coupling the second land to the second terminal; and

a die comprising first and second power supply nodes coupled to the first and second lands, respectively.

12. The electronic assembly recited in claim 11, wherein the substrate further comprises a second plurality of lands on a second surface thereof, including a third land coupled to the first terminal and a fourth land coupled to the second terminal.

13. The electronic assembly recited in claim 12, wherein the pitch of the second plurality of lands is greater than the pitch of the first plurality of lands, and wherein the pitch is increased within the organic layer.

14. The electronic assembly recited in claim 12, wherein the first plurality of lands further comprises a fifth land coupled to a signal node of the die, and wherein the second plurality of lands comprises a sixth land coupled to the fifth land via a conductive path that comprises one of the plurality of conductors.

15. The electronic assembly recited in claim 14, wherein the pitch of the second plurality of lands is greater than the pitch of the first plurality of lands, and wherein the pitch is increased within the organic layer.

16. The electronic assembly recited in claim 12, wherein the third and fourth lands are positioned to be coupled to corresponding power supply nodes of an additional substrate subjacent to the multilayer ceramic substrate.

17. The electronic assembly recited in claim 11, wherein the capacitor comprises a plurality of high permittivity layers.

18. The electronic assembly recited in claim 17, wherein the capacitor comprises a plurality of conductive layers interleaved with the high permittivity layers, such that alternating conductive layers are coupled to the first and second lands, respectively.

19. The electronic assembly recited in claim 11, wherein the organic portion comprises a plurality of layers, each comprising a portion of the plurality of conductors.

20. An electronic system comprising an electronic assembly having a die with first and second power supply nodes coupled to a multilayer substrate, wherein the substrate comprises:

a ceramic portion comprising at least one embedded capacitor having first and second plates;

a first plurality of lands on a first surface thereof, including a first land coupled to the first power supply node, and a second land coupled to the second power supply node; and

an organic portion comprising a plurality of conductors, including first and second conductors respectively coupling the first land to the first plate and coupling the second land to the second plate.

21. The electronic system recited in claim 20, wherein the substrate further comprises a second plurality of lands on a second surface thereof including a third land coupled to the first plate and a fourth land coupled to the second plate, wherein the pitch of the second plurality of lands is greater than the pitch of the first plurality of lands, and wherein the pitch is increased within the organic layer.

22. The electronic system recited in claim 21, wherein the first plurality of lands further comprises a fifth land coupled to a signal node of the die, and wherein the second

plurality of lands comprises a sixth land coupled to the fifth land via a conductive path that comprises one of the plurality of conductors.

23. The electronic system recited in claim 22, wherein the pitch of the second plurality of lands is greater than the pitch of the first plurality of lands, and wherein the pitch is increased within the organic layer.

24. The electronic system recited in claim 20, wherein the organic portion comprises a plurality of layers, each comprising a portion of the plurality of conductors.

25. A data processing system comprising:
a bus coupling components in the data processing system;
a display coupled to the bus;
external memory coupled to the bus; and
a processor coupled to the bus and comprising an electronic assembly including:
a die comprising first and second power supply nodes and a first signal node; and
a multilayer substrate comprising:
a ceramic portion comprising a second signal node and at least one embedded capacitor having a first terminal and a second terminal; and
an organic portion comprising a plurality of conductors, including a first conductor coupling the first power supply node to the first terminal, a second conductor coupling the second power supply node to the second terminal, and a third conductor coupling the first signal node to the second signal node.

26. The data processing system recited in claim 25, wherein the plurality of conductors are fanned out within the organic portion.

27. The data processing system recited in claim 25, wherein the organic portion comprises a plurality of layers, each comprising a portion of the plurality of conductors.

28. A method for making a substrate to package a die, the method comprising:

forming a first portion of the substrate using ceramic materials, the first portion comprising at least one capacitor having first and second terminals;

forming a second portion of the substrate using organic materials, the second portion comprising a plurality of conductors therein, including a first conductor coupled to the first terminal and a second conductor coupled to the second terminal; and

forming a first plurality of lands on a surface of the second portion of the substrate, including a first land coupled to the first conductor, and a second land coupled to the second conductor, wherein the first and second lands are positioned to be coupled to first and second power supply nodes of the die.

29. The method recited in claim 28, wherein forming the first portion comprises forming a first signal node, wherein forming the second portion comprises forming a third conductor coupled to the first signal node, and wherein forming the first plurality of lands comprises forming a third land coupled to the third conductor, the third land being positioned to be coupled to a signal node of the die.

30. The method recited in claim 28 and further comprising:

forming a second plurality of lands on a surface of the first portion of the substrate, including a third land coupled to the first terminal, and a fourth land coupled to the second terminal, and wherein forming the second portion comprises fanning out the plurality of conductors from a first pitch of the first plurality of lands to a second pitch of the second plurality of lands.